CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-18 (Cancelled)

19. (New) A method of managing a memory bus, the method comprising:

receiving a first memory access request from a first request agent that represents a first functional device and a second memory access request from a second request agent that represents a second functional device;

loading a first access priority value into a first counter timer, wherein the first access priority value corresponds to a processing function that is provided by the first functional device;

loading a second access priority value into a second counter timer, wherein the second access priority value corresponds to a different processing function that is provided by the second functional device;

wherein the first functional device accesses a memory bus before the second functional device when the first access priority value represents a higher priority than the second access priority value; and

wherein the second functional device accesses the memory bus before the first functional device when the second access priority value represents a higher priority than the first access priority value.

20. (New) The method of Claim 19, wherein a bus elector compares the first access priority value to the second access priority value.

21. (New) The method of Claim 19, wherein the first access priority value represents the higher priority when the first access priority value is greater than the second access priority value.

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22. (New) The method of Claim 19, wherein the first access priority value represents the higher priority when the first access priority value is lower than the second access priority value.

23. (New) The method Claim 22, further comprising:

starting a first clock cycle when the first functional device accesses the memory bus; and

decrementing the second access priority value after the first clock cycle has expired.

24. (New) The method of Claim 23, further comprising:

receiving a third memory access request from a third request agent that represents a third functional device;

loading a third access priority value into a third counter timer, wherein the third access priority value corresponds to another processing function that is provided by the third functional device;

wherein the second functional device has priority access to the memory bus when the decremented second access priority value represents a higher priority than the third access priority value; and

wherein the third functional device has priority access to the memory bus when the third access priority value represents a higher priority than the decremented second access priority value.

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25. (New) The method of Claim 24, further comprising:

decrementing the third access priority value, when the second functional device accesses the memory bus and a second clock cycle ends;

receiving a next memory access request from the second request agent;

resetting the decremented second has priority access to priority value to the second access priority value; and

wherein the second functional device has priority access to the memory bus when the second access priority value represents a higher priority than the decremented third access priority value; and

wherein the third functional device accesses the memory bus when the decremented third access priority value represents a higher priority than the second access priority value.

26. (New) The method of Claim 19, further comprising:

determining whether the memory bus is locked; and

preventing the first functional device and the second functional device from accessing the memory bus when the memory bus is locked.

27. (New) The method of Claim 19, wherein the first priority access value and the second priority access value are stored in a control register.

28. (New) The method of Claim 27, further comprising dynamically adjusting the first priority access value and the second priority access value in response to a user request.

29. (New) A system to manage a memory bus, the system comprising:

a memory bus configured to communicate with a first functional device that provides a first processing function and with a second functional device that provides a second processing function;

wherein the first functional device is represented by a first request agent and the second functional device is represented by a second request agent;

a control register configured to store a first access priority value associated with the first request agent and a second access priority value associated with the second request agent;

wherein the first access priority value corresponds to the first processing function and the second access priority value corresponds to the second processing function;

a control unit configured to load the first access priority value into a first counter timer when the first request agent issues a first memory access request, and to load the second access priority value into a second counter timer when the second request agent issues a second memory access request;

wherein the first functional device accesses the memory bus before the second functional device when the first access priority value represents a higher priority than the second access priority value; and

wherein the second functional device accesses the memory bus before the first functional device when the second access priority value represents a higher priority than the first access priority value.

30. (New) The system of Claim 29, wherein the first memory access request and the second memory access request are received by a bus arbiter.

31. (New) The system of claim 29, further comprising a bus elector coupled to the first counter timer and the second counter timer, wherein the bus elector is configured to compare the first access priority value to the second access priority value.

32. (New) The system of claim 29, wherein the first functional device and the second functional device are included within a moving picture experts group (MPEG) video codec processor.

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33. (New) The system of claim 29, further comprising a control unit coupled to the request agents for respectively receiving corresponding requests for access to the memory bus.

34. (New) The system of claim 29, wherein the first functional device and the second functional device are selected from a group consisting of memory controllers, image processors, motion estimation processors, and host/peripheral interfaces.

35. (New) The system of claim 29, wherein the first access priority value represents a first maximum latency count and the second access priority value represents a second maximum latency count.

36. (New) The system of Claim 29, further comprising a plurality of clocks that time a clock cycle when the memory bus is accessed.

37. (New) The system of claim 36, further comprising a bus release mechanism, wherein the plurality of clocks begin the clock cycle when the bus release mechanism releases the first functional device or the second functional device to access the memory bus.

38. (New) The system of claim 36, further comprising a bus release mechanism, wherein the bus release mechanism releases the first functional device or the second functional device to access the memory bus after at least one of the plurality of clocks begin to time the clock cycle.